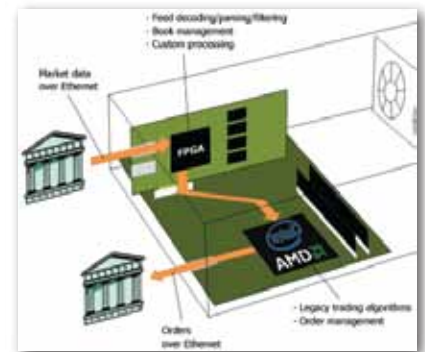


The Accelize FPGA-based smart feed handlers enable the acceleration of financial trading platforms, and are especially aimed at high-frequency trading, ultra-low latency feed handling, and real-time algorithmic trading.

Our smart feed handlers' solution framework includes a combination of hardware, firmware, and software, each provided with different options to fit specific acceleration requirements.



Example: "Ticker Plant" Acceleration Platform

Hardware Platforms

XP4S530LP-20G

- Low profile PCIe 2.0 (Gen2) x8
- Dual 10G or dual 1G Ethernet
- 2GB DDR3 SDRAM
- 36MB QDRII+ SRAM

XP4S1050GT-20G

- Dual FPGA
- PCIe 2.0 (Gen2) x8
- Dual 10G Ethernet
- 1GB DDR3 SDRAM

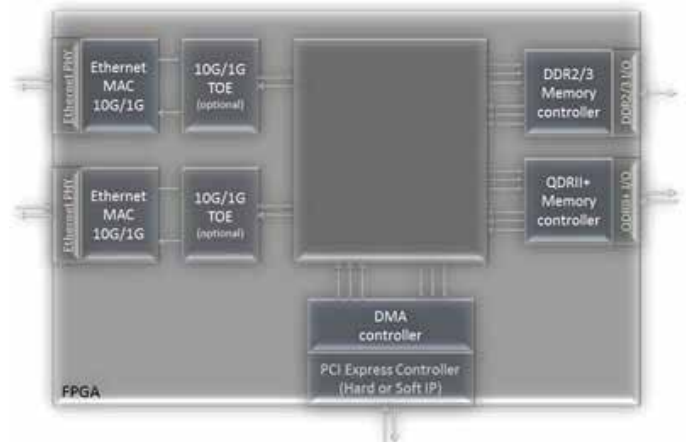
XP4S1050-10G

- Dual FPGA
- PCIe 2.0 (Gen2) x4
- 10G Ethernet
- 1GB DDR3 SDRAM

Firmware Environment

We offer a complete IP infrastructure that enables near instant access to market data, with 70ns Ethernet MAC latency, 200ns Ethernet MAC + TOE latency, and under 50ns PCI Express + DMA latency at Gen2 speeds.

- Framework #1:
 - 10G or 1G Ethernet MAC
 - PCIe multi-channel DMA controller
 - Memory controllers
- Framework #2:
 - 10G or 1G Ethernet MAC
 - 10G or 1G Traffic Offload Engine (TOE) (Up to 32 sessions)
 - PCIe multi-channel DMA controller
 - Memory controllers



Infrastructure Software

The Accelize solution includes a latency optimized PCIe device driver for 32-bit and 64-bit Linux distributions.

A C/C++ API provides application software with easy to use higher-level functions to access hardware resources.

Productivity Software

Our Hardware Compile Environment "HCE" allows our FPGA accelerator cards to be programmed using C/C++.

HCE automatically generates the interfaces and control logic that enables HCE-compiled algorithms to connect seamlessly with the FPGA's IP infrastructure.